**Refer to PL part inputs**.

FPGA SPECIFICATIONS

**Lior Yosef**

Date 22-01-2024

2024

Contents

[ON COMMAND 2](#_Toc157081372)

[STATUS MESSAGAE 2](file:///D:\EDM_Workspace\Elop_CondorMS_C10A\Elop_CondorMS_C10A_SBC_Board\R01A\Doc\FPGA%20specifications.docx#_Toc157081373)

[ENABLE POWER SUPPLIES 4](#_Toc157081376)

[STATUS MESSAGAE 6](#_Toc157081377)

[Voltage RMS Calculations 8](#_Toc157081378)

[Current RMS Calculations 9](#_Toc157081379)

[I\_sns 9](#_Toc157081380)

[Current Calculations 10](#_Toc157081381)

[Current offset measurement 11](#_Toc157081382)

[Current offset Calculations 12](#_Toc157081383)

[**FAN Control** 13](#_Toc157081384)

[SHUTDOWN\_OUT\_FPGA 13](#_Toc157081385)

[ESHUTDOWN\_OUT\_FPGA 13](#_Toc157081386)

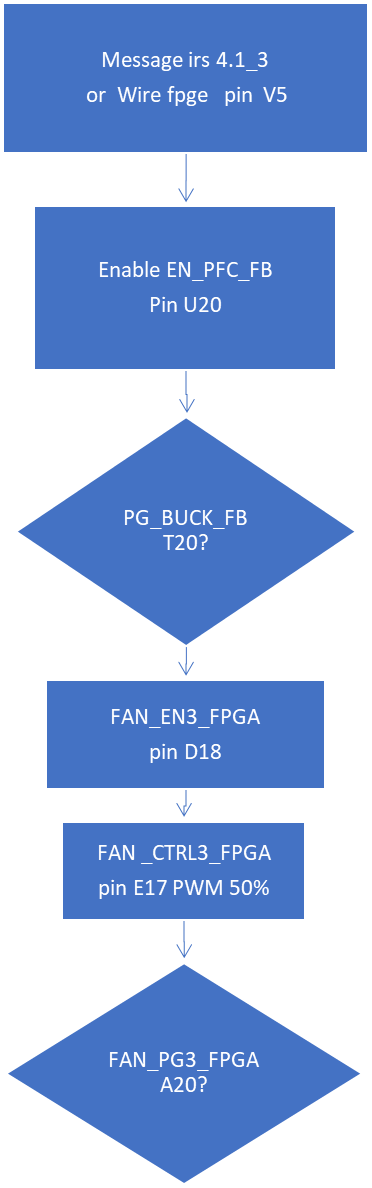
[RESET\_OUT\_FPGA 13](#_Toc157081387)

[VCC\_12V\_REDUNDANT POWER DOWN ALARM 14](#_Toc157081388)

[POD STATUS FPGA(LOW) CHECK USING LAMP STATUS 15](#_Toc157081389)

[POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS 16](#_Toc157081390)

# ON COMMAND



refer to  **FAN Control**

# [STATUS MESSAGAE](#_STATUS_MESSAGAE)

FAN\_EN2\_FPGA

FAN\_EN1\_FPGA

YES

## [POD STATUS FPGA(LOW) CHECK USING LAMP STATUS](#_POD_STATUS_FPGA)

## [POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS](#_POD_STATUS_FPGA(HIGH))

NO

Output 1KHZ 50%

FB\_PG1   
FB\_PG2

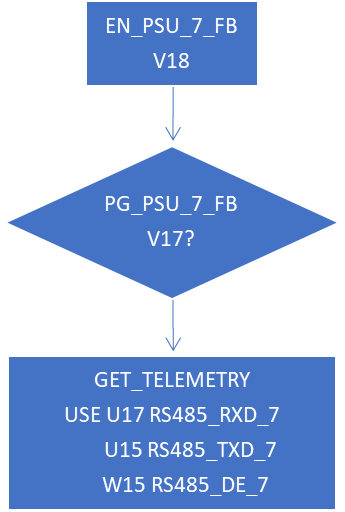
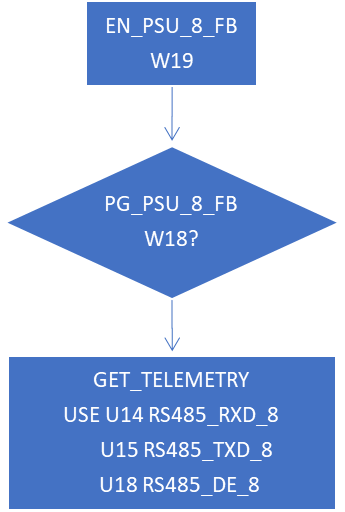
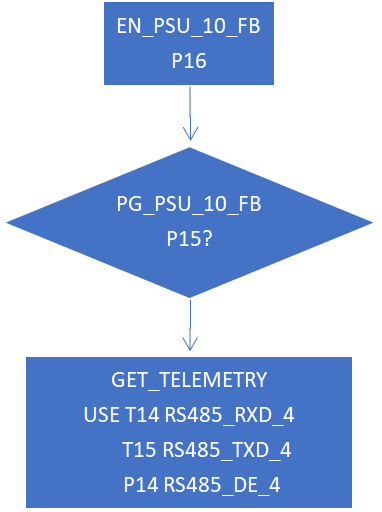
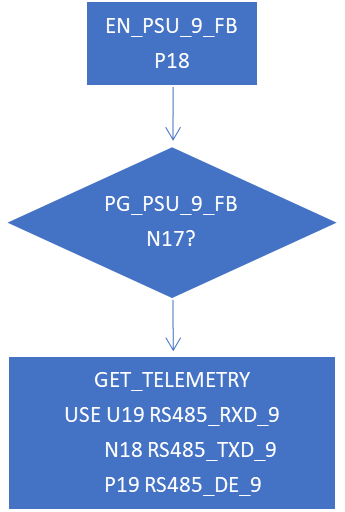
FB\_PG3

F

[CONTINUE TO ENABLE POWER SUPPLIES](#_ENABLE_POWER_SUPPLIES)

CONTINUE TO ENABLE FAN

# ENABLE POWER SUPPLIES



BUCK

USE V13 RS485\_RXD\_3

V12 RS485\_TXD\_3

W13 RS485\_DE\_3

**1msec after**

**All PG are ON:**

CCTCH\_INH\_FPGA G19

ECTCH\_INH\_FPGA H20

Go ON

# STATUS MESSAGAE

POD\_STATUS\_FPGA G17

Refer 3.1.6

LAMP\_STATUS\_FPGA J15

INPUT: if POD\_STATUS\_FPGA is HIGH

LAMP\_STATUS\_FPGA should be HIGH else 🡪 ERROR

# Voltage RMS Calculations

result 🡪 Vsns\_PH1, Vsns\_PH2, Vsns\_PH3

Sample frequency = 10kHz (AC FREQUENCY=400Hz, samples number=25, minimum samples number is 20)

CODE:

for (I=0; I<25; I++)

If (result>2048) {

sum+=new result

}

else {

sum+=new result

}

Rms input voltage =

**The result unit is VOLT.**

**1 - LSB = 0.109 Volt**

**==================================**

# Current RMS Calculations

# I\_sns

# Current Calculations

Offset🡪 every input has its offset calculated. see **Current offset measurement**

result 🡪 PH1\_I\_sns, PH2\_I\_sns, PH3\_I\_sns, DC\_PWR\_I\_sns

N 🡪 samples number

Sample frequency = 10kHz (AC FREQUENCY=400Hz, minimum samples number is 20)

CODE:

for (I=0;I<25;I++)

If (result>offset) {

sum+=new result

}

else {

sum+=new result

}

Rms input current =

**The result unit is Amper.**

**1 - LSB = 0.0147Amper**

# Current offset measurement

# 

Frequency 1kHz

## Current offset Calculations

Offset🡪 every input has its offset just as it read

result 🡪 PH1\_ZCR\_sns, PH2\_ZCR\_sns, PH3\_ZCR\_sns, DC\_PWR\_ZCR\_sns

no calculation is needed.

CODE:

result offset = result (the raw data)

# FAN Control

There are three Fans. Each Fan need enable signal FAN\_EN1, FAN\_EN2, FAN\_EN3

FAN speed is controlled by FAN\_CTRL FAN\_CTRL1.FAN\_CTRL2, FAN\_CTRL3

FAN\_CTRL is square wave at 1Khz with duty cycle TBD (let’s start with 50%)

The FANS actual SPEED IS feedback by hall effect signal FAN\_HAAL1\_FPGA, FAN\_HALL2\_FPGA, FAN\_HALL3\_FPGA.

The hall1,2,3 frequency is equal to the FAN speed, and it is measure and compare to a fix value which is TBD.

In case the speed (hall frequency) is out of the desired operation range the CTRL duty cycle is increased or decreased in purpose we need to increase or decrease the FAN speed.

Each Fan has a different speed.

All values will be declared after FAN integration.

SHUTDOWN\_OUT\_FPGA G15

Refer to 3.1.5.2 for shutdown when system power of (named power down)

Refer to 3.2.10.2.1 to create shut down in over voltage for input voltage.

Refer to 3.2.10.5 to create shut down in over temperature.

ESHUTDOWN\_OUT\_FPGA K14

Refer to 3.2.10.2 for the case of outputs over voltage.

RESET\_OUT\_FPGA H15   
 refer to 3.1.5.1 System Reset (“short” reset)

## VCC\_12V\_REDUNDANT POWER DOWN ALARM

100Hz sampling

NO

YES

NO

YES

## POD STATUS FPGA(LOW) CHECK USING LAMP STATUS

NO

## [POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS](#_POD_STATUS_FPGA(HIGH)_1)

NO

YES

YES

## POD STATUS FPGA(HIGH) CHECK USING LAMP STATUS

CHECK 3 TIMES